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SEMICONDUCTOR CHIP CAPABLE OF IMPLEMENTING WIRE BONDING OVER ACTIVE CIRCUITS

Abstract

An integrated circuit including a reinforced bonding pad structure is disclosed. The reinforced bonding pad structure includes a bondable metal layer defined on a stress-buffering dielectric layer, and an intermediate metal layer damascened in a first inter-metal dielectric (IMD) layer disposed under the stress-buffering dielectric layer. The intermediate metal layer is situated directly under the bondable metal layer and is electrically connected to the bondable metal layer with a plurality of via plugs integrated with the bondable metal layer. At least one metal frame is damascened in a second IMD layer under the first IMD layer. The metal frame is situated directly under the intermediate metal layer for counteracting mechanical stress exerted on the bondable metal layer during bonding. An active circuit portion including active circuit components of the integrated circuit is situated directly under the metal frame of the reinforced bonding pad structure.